Remarks

The examiner's further reconsideration of the application is requested in view of the simple amendment to claim 1 above, and comments which follow.

In the office action, the examiner continues to reject the claims, with claims 1, 7, 8 and 10 being rejected by the examiner under 35 U.S.C. §102 as being anticipated by Chi U.S. Patent Number 5,608,243, and claims 6 and 9 being rejected by the examiner under 35 U.S.C. §103 as being unpatentable over Chi in view of Takemoto U.S. Patent Number 4,148,048. Reconsideration is again requested.

The Examiner still alleges that the channel region in Chi does not store carriers but only transports carriers in between an image collection region and a source region.

The applicant respectfully submits that this is not correct.

In Chi, prior to integration, voltages are applied such that a conductive channel is formed between p+region 114 and substrate 110, so as to reset the voltage on p+region 114 and floating gate 116 (col.3 lines 30-45). Thereafter, the voltage on the reset gate is changed, and the formed conductive channel is eliminated (col.3 lines 46-50).

During an integration period, photons strike the surface of the p+region 114, and as a result create a number of electron-hole pairs (col.3 lines 55-60). The electrons are swept to the drain region 108, the holes are swept into the p+region 114 (col.3 lines 61-67).

It is only after the integration period (col. 4 line 7), when a voltage Vread is applied for reading out the charges, that the formation of a conductive channel is induced on the top surface of the channel region of the substrate. It is this conductive channel which allows a current to flow from the drain region to the source region (col.4 lines 7-14). This means that during the integration period, when Vread does not induce a conductive channel on the top surface of the

channel region of the substrate, charges cannot flow from the drain region to the source region. This means that the charges generated in the junction between p+region 114 and drain region 108 must be stored, during the integration period, in the path between where they are being generated and where they are being collected by the source region. The only path between those two locations is the channel region. Therefore, the channel region stores carriers during the integration period.

In the present invention, during an integration period, charges are stored at the end of their path only, in the doped region where they can be read out, and not in the planar current flow carrier transport pathway from or through the collection region to the doped or inverted region. In Chi, to the contrary, first collection and storing takes place, and only at the moment of readout (when a suitable voltage Vread is applied), carriers are transported finally up to the readout region (source). This is a fundamental difference between the present invention and the prior art: according to the present invention charges are only stored at the end readout location, in Chi charges are stored in an intermediate location which is different from the readout location.

Nevertheless, in order to unquestionably distinguish the claims presently on file, and in order to better distinguish over Chi, a slightly amended claim 1 is set forth above. This claim now states that carriers are not stored in the carrier transport pathway during an image integration period. This distinguishes the present invention over Chi where, as already stated above, carriers are stored during the integration period, as carriers only flow to the source at the moment a suitable readout voltage has been applied.

As amended claim 1 is considered to be novel and non-obvious, dependent claims 6 to 10 are considered patentable as well by virtue of their dependence from claim 1.

Further and favorable reconsideration of the application is therefore urged.

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Respectfully submitted,

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